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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,132	06/23/2000	Brian A. Vaartstra	150.00650102	3538

7590 01/07/2005

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EXAMINER	
LEE, EUGENE	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/603,132	VAARTSTRA ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *45-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *45-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 45 thru 48, 50, and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsubara et al. 5,122,923. Matsubara discloses (see, for example, Fig. 1) a capacitor (semiconductor device structure) comprising a silicon substrate (substrate assembly including a surface) 1 and a lower electrode (diffusion barrier layer) 3. In column 4, lines 24-27, Matsubara discloses the lower electrode being made of layers of ruthenium, ruthenium oxide, ruthenium silicide and stacked structures.

Regarding claim 48, see aluminum electrode (one or more additional conductive layers) 5.

Regarding claims 50 and 51, Matsubara discloses (see, for example, Fig. 1 and column 3, lines 43-47) a capacitor structure comprising a lower electrode (first electrode) 3, dielectric layer (high dielectric material) 4, and upper electrode (second electrode) 5.

3. Claims 45, 46, 50, and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuroiwa et al. 6,239,460 B1. Kuroiwa discloses (see, for example, Fig. 10 and column 13, lines 12-14) a semiconductor device structure comprising a substrate (substrate assembly) 101 and a ruthenium silicide layer (diffusion barrier layer) 132.

Regarding claims 50 and 51, Kuroiwa discloses (see, for example, FIG. 10) a capacitor structure comprising a metal electrode (first electrode) 130/132, capacitor dielectric 115 and upper electrode (second electrode) 116. In column 13, lines 11-15, Kuroiwa discloses the ruthenium silicide layer 132 is formed from a portion of metal electrode 130.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 48, 49, and 54 thru 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroiwa et al. '460 B1 as applied to claims 45, 46, 50, and 51 above, and further in view of Aoyama et al. 5,852,307. Kuroiwa does not disclose a silicon containing region. However, it was well known in the art to use a substrate made of silicon (silicon containing region). Aoyama discloses (see, for example, FIG. 21D and column 15, lines 58-60) a capacitor structure on a silicon substrate 101. It would have been obvious to one of ordinary skill in the art at the time of invention to use a silicon containing region (making the substrate of Kuroiwa a silicon substrate) in order to form a semiconductor device and form diffused regions therein, and since it has been

held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims 48 and 49, see FIG. 10 wherein Kuroiwa discloses a metal electrode (one or more additional conductive layers) 130 and column 9, lines 39-42 wherein Kuroiwa discloses the metal electrode comprising ruthenium (Ru) or iridium (Ir).

Regarding claim 54, Kuroiwa discloses (see, for example, FIG. 10) a DRAM (integrated circuit structure) comprising a substrate assembly including a substrate (silicon containing region) 101, transfer gate transistor (active device) 103b, and a plug (interconnect) 111 including a ruthenium silicide layer 132.

Regarding claim 56, Kuroiwa discloses a metal electrode (conductive contact material) 130.

Regarding claims 58-62 and 64-68, Kuroiwa discloses the ruthenium silicide layer (conformal layer) 132 within an opening of the insulating film 110. The aspect ratio (ratio of height to width) is clearly greater than 1.

Regarding claim 63, Kuroiwa discloses (see, for example, FIG. 10) a capacitor comprising a metal electrode (first electrode) 130, capacitor dielectric film (high dielectric material) 115, upper electrode (second electrode) 116, and ruthenium silicide layer (diffusion barrier layer) 132.

6. Claims 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroiwa et al. '460 B1 in view of Aoyama et al. '307 as applied to claims 48, 49, and 54-68

above, and further in view of Matsubara et al. 5,122,923. Kuroiwa in view of Aoyama does not disclose the first electrode comprising one or more additional conductive layers. However, it was well known in the art at the time of invention to use multiple layers in the electrodes of a capacitor. In column 4, lines 25-27, Matsubara discloses a lower electrode comprising multiple layers of ruthenium, ruthenium oxide, ruthenium silicde and stacked structures consisting of these materials. It would have been obvious to one of ordinary skill in the art at the time of invention to have the first electrode comprising one or more additional conductive layers in order to form a bottom electrode, and since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis paper Co. vs. Bemis Co., 193 USPQ 8.

Product-by-Process Limitations

7. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law

makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

The limitation "chemical vapor codeposited" merely recites a method of forming and does not deviate from the **structure of a diffusion barrier made of $RuSi_x$**.

Response to Arguments

8. Appellant's arguments filed 10/4/04 have been fully considered but they are not persuasive.

The gist of the appellant's arguments against the anticipatory rejection is primarily based on the method used to form a diffusion barrier of $RuSi_x$ in a semiconductor device structure. However, the method (chemical vapor codeposition) is not germane to the claims being examined in the instant application. That is, because the invention, as set forth in the claims, is clearly directed towards an apparatus. Therefore the method of making the invention does not structurally distinguish the claimed invention from the cited prior art.

On page 10, paragraph 2 of appellant's amendment and response filed 10/4/04

, the appellant argues that the diffusion barrier layer made by a method of "chemical vapor codeposition" is different than the layer made by a method of "sputtering". However, the claims, as presented in the instant application, do not state any of these structural differences. The claims only state a diffusion barrier made by a method of chemical vapor deposition and do not state at all any structural limitations that may or may not be attributed to this method. It is the claims that define a claimed invention and the appellant has not stated any of these structural limitations in the claims. On page 10, paragraph 3 of the appeal brief, the appellant has referred

to a "Declaration Under 37 C.F.R. 1.132" (filed 1/27/03) that states structural differences between a sputter coating diffusion barrier layer and a chemical vapor deposited diffusion barrier layer that the appellant believe are true. However, the appellant has provided no scientific evidence to support the statements in the Declaration. The statements in the Declaration are conclusionary in nature and since the appellant has provided no factual evidence to back them up, the statements carry little weight. However, for the sake of completeness, the appellant's Declaration is assessed herein.

In paragraph 8 of the Declaration, appellant states that a sputter coated layer, with respect to high aspect ratio structures, provides different coverage thereon when compared to a chemical vapor deposited layer. Appellant further argues that a chemical vapor deposited film provides a highly conformal layer within deep contacts and other openings such as for lower electrodes of storage cell capacitors and these highly conformal layers relative to high aspect ratio structures are generally not possible with sputter coating. However, the appellant's claims do not state high aspect ratio structures or deep contacts such that a different structure from chemical vapor deposition could possibly occur. The appellant's argument that a different structure will occur because of high aspect ratio structures or deep contacts is moot here because there are no high aspect ratio structures or deep contacts limitations in the present claims. Therefore, whether the layer is laid down by chemical vapor deposition or sputtering in Matsubara's invention is irrevelant to the instant claims. In any event, a method of sputtering would also form a conformal layer on a substrate and therefore the layer would have the same structure whether laid down by sputtering or chemical vapor deposition.

On page 11, third paragraph, the appellant states that a sputter coated diffusion barrier layer "may" have surface damage by the implantation of a metal. However, this is hypothetical and it can equally be said that the sputter coated diffusion barrier layer "may not" have surface damage. The Declaration is of little probative value on this issue. Since Matsubara discloses a simple diffusion barrier layer 3 on a flat surface, it would be reasonable to assume that in such a simple structure, no surface damage would occur to the diffusion barrier layer. Further, Matsubara discloses (see, for example, FIG. 1) a silicon oxide layer 2 in between the substrate 1 and lower electrode 3. It is physically not possible that a metal such as ruthenium that is used to form the lower electrode 3 can implant into the substrate when there is a silicon oxide layer covering the substrate. The appellant further states that silicon can be implanted into platinum surfaces during sputter coating of $RuSi_x$, where the silicon can diffuse into the platinum containing substrate. However, Matsubara makes no reference to platinum in his invention.

On page 13, second paragraph, the appellant states the Kuroiwa discloses many structural differences over a ruthenium silicide layer formed by silicidation. Again, the method in which the invention is made is not an issue with respect to the rejection of the claims. However, this argument will be addressed since it is related to the structural limitations regarding the diffusion barrier layer being formed of $RuSi_x$. The appellant states that chemical vapor codeposited $RuSi_x$ layer includes a more uniform distribution of silicon throughout the layer, whereas a silicidated ruthenium silicide layer exhibits a gradient of silicon content from the ruthenium/silicon interface to the opposite surface of the ruthenium layer and further a silicidated ruthenium silicide layer may include uneven island formations of silicide instead of a more uniform $RuSi_x$ formed by chemical vapor codeposition. However these statements are not supported by any

evidence on the part of the appellant and are not even addressed in the Declaration. These statements are only conjecture on part of the appellant. Kuroiwa simply states a ruthenium silicide layer 132 in between a plug 111 and metal electrode 130. Kuroiwa makes no mention of a "gradient of silicon content" or "uneven island formation of silicide" but only a uniform ruthenium silicide on top of a metal electrode 130.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

Eugene Lee
January 4, 2005

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